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FLUX Encoders
Interface Guide

Technical Datasheet

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www.flux.gmbh

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1. Selection Matrix

1.1. Terms and definitions

Interface type:

1. A **serial synchronous** interface for a position encoder is a communication method that transmits data in a synchronized manner, typically using a clock signal to ensure that data is transferred at a consistent rate.
2. A **serial asynchronous** interface doesn't rely on a synchronized clock signal and transmits data without strict timing requirements.
3. A **quadrature interface** employs two electrical signals, "A" and "B", with a 90-degree phase difference. As the encoder rotates or moves, these channels produce a sequence of pulses with each pulse representing a specific degree of movement. Additionally the "Z" signal provides a reference point for precise position determination..

Line compensation:

Line delay compensation in a serial interface refers to techniques used to mitigate the impact of varying signal propagation delays along the transmission medium. It ensures that data signals arrive at their intended destination in a synchronized manner, despite differences in the time it takes for these signals to traverse the transmission path. To utilize these capabilities, the encoder must have built-in support for them, and the master module within the motion controller must also incorporate the necessary implementation.

Register access:

Register access in a serial interface like BiSS-C refers to the ability to read from or write to specific registers within the device's memory space via the interface. These registers often store configuration settings, status information, or control parameters, allowing users to customize and monitor the behavior of the connected device.

Multi-turn support:

Multi-turn support in a serial interface allows the interface to accurately track and communicate the number of complete revolutions or rotations made by an encoder, beyond a single turn. It ensures that the interface can handle and transmit data representing multiple full rotations.

It's important to emphasize that the multi-turn feature can be applied even to encoders that aren't inherently multi-turn. We recommend thoroughly reviewing the documentation, and if any questions or uncertainties arise, don't hesitate to reach out for clarification and guidance.

1.2. Rotary Encoders: Interfaces for absolute position

Interface		Line Compensation	Register support	Multi-Turn Support	Link to Chapter
Serial Synchronous Interface					
BiSS-C	**BIS10**	✓	✓	✗	Chapter 2.2.
	BIS20	✓	✓	✗	Chapter 2.3.
	BIS21	✓	✓	✓	Chapter 2.3.
	BIS00	✓	✓	✗	Chapter 2.1.
SSI	**SSI00**	✗	✗	✗	Chapter 3.1.
	SSI01	✗	✗	✗	Chapter 3.2.
	SSI02	✗	✗	✗	Chapter 3.3.
	SSI03	✗	✗	✓	Chapter 3.4.
	SSI04	✗	✗	✗	Chapter 3.5.
Serial Asynchronous Interface					
UART	**UAT00**	**N/A**	✗	✗	Chapter 4.1.
	UAT01	**N/A**	✗	✗	Chapter 4.1.

1.3. Linear Encoders: Interfaces for absolute position

Interface		Line Compensation	Register support	Link to Chapter
Serial Synchronous Interface				
BiSS-C	**BIS00**	✓	✓	Chapter 2.1.
SSI	**SSI00**	✗	✗	Chapter 3.1.

1.4. Rotary Encoders: Interfaces for incremental position

Interface		Line Compensation	Register support	Multi-Turn Support	Link to Chapter
Serial Synchronous Interface					
SSI	**SSI20**	✗	✗	✗	Chapter 3.6.
Quadrature interface					
A/B/Z	**INC00**	**N/A**	✗	✗	Chapter 4.1.
	INC01	**N/A**	✗	✗	Chapter 4.1.
	INC02	**N/A**	✗	✗	Chapter 4.1.
	INC03	**N/A**	✗	✗	Chapter 4.1.

1.5. Linear Encoders: Interfaces for incremental position

Interface		Line Compensation	Register support	Link to Chapter
Serial Synchronous Interface				
SSI	**SSI20**	✗	✗	Chapter 3.6.
Quadrature interface				
A/B/Z	**INC00**	**N/A**	✗	Chapter 4.1.
	INC01	**N/A**	✗	Chapter 4.1.
	INC02	**N/A**	✗	Chapter 4.1.
	INC03	**N/A**	✗	Chapter 4.1.

2. BiSS-C Interfaces

2.1. BIS00: Serial interface *BiSS-C*

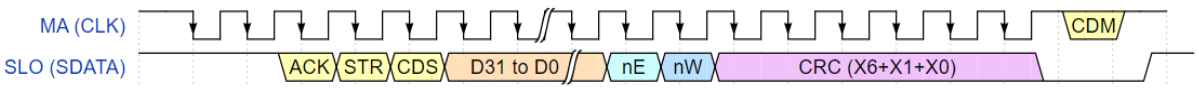
The BIS00 serves as an implementation of the bidirectional *BiSS-C* ® interface (a registered trademark of IC-Haus GmbH) and boasts the following key features:

- it reserves 32 bits for encoder position data
- the encoder position data is right-aligned, with unused upper bits/MSB set to 0

While the BIS00 is a suitable choice for linear encoders, it's important to note that compatibility issues with certain motion controllers may arise when used with rotary encoders. In such cases, we strongly recommend considering the BIS10 or BIS20 interface for rotary encoders.

Parameter	Note	Min.	Typ.	Max.	Unit
Clock frequency	data updated on rising clock edge	0.1		5.0	MHz
Processing time	ACK bit length = 1 clock (real time encoder)		0		µs
Total number of bits	incl. Position, Status, CRC bits		40		bits
Position bits (D31..D0)	**Right** aligned, unused MSB set 0		32		
Status bits	nE - not Error, active low nW - not Warning, active low		2		bits
CRC bits	Polynome: 0x43 ($X^6+X^1+X^0$) Start value: 0x00 Inverted before transmission		6		bits

The update of serial data occurs following the rising edge of the clock signal, and the bit must be latched at the subsequent falling edge of the clock signal. Position latching initiates with the first falling edge of the clock signal.



Time diagram for interface BIS00

It's worth noting that the BiSS-C specification provides comprehensive guidelines on line delay compensation, particularly useful for lengthy cable connections, allowing for adjustment in the timing of bit latching. For more detailed information, please refer to the official BiSS-C specification in Chapter "Line Delay" at the following link: https://biss-interface.com/.

2.2. BIS10: Serial interface *BiSS-C*

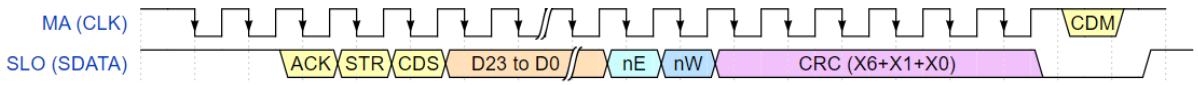
The BIS10 serves as an implementation of the bidirectional *BiSS-C* ® interface (a registered trademark of IC-Haus GmbH) and boasts the following key features:

- it reserves 24 bits for encoder position data
- the encoder position data is left-aligned, with unused lower bits/LSB set to 0

BIS10 is the recommended choice for rotary encoders with a resolution of up to 24 bits.

Parameter	Note	Min.	Typ.	Max.	Unit
Clock frequency	data updated on rising clock edge	0.1		5.0	MHz
Processing time	ACK bit length = 1 clock (real time encoder)		0		µs
Total number of bits	incl. Position, Status, CRC bits		32		bits
Position bits (D23..D0)	**Left aligned**, unused LSB set 0		24		
Status bits	nE - not Error, active low nW - not Warning, active low		2		bits
CRC bits	Polynome: 0x43 ($X^6+X^1+X^0$) Start value: 0x00 Inverted before transmission		6		bits

The update of serial data occurs following the rising edge of the clock signal, and the bit must be latched at the subsequent falling edge of the clock signal. Position latching initiates with the first falling edge of the clock signal.



Time diagram for interface BIS10

It's worth noting that the BiSS-C specification provides comprehensive guidelines on line delay compensation, particularly useful for lengthy cable connections, allowing for adjustment in the timing of bit latching. For more detailed information, please refer to the official BiSS-C specification in Chapter "Line Delay" at the following link: https://biss-interface.com/.

2.3. BIS20: Serial interface *BiSS-C*

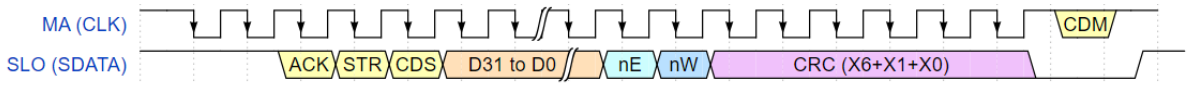
The BIS20 serves as an implementation of the bidirectional *BiSS-C* ® interface (a registered trademark of IC-Haus GmbH) and boasts the following key features:

- it reserves 32 bits for encoder position data
- the encoder position data is left-aligned, with unused lower bits/LSB set to 0

BIS20 is the recommended choice for rotary encoders with a resolution starting with 25 bits and higher.

Parameter	Note	Min.	Typ.	Max.	Unit
Clock frequency	data updated on rising clock edge	0.1		5.0	MHz
Processing time	ACK bit length = 1 clock (real time encoder)		0		µs
Total number of bits	incl. Position, Status, CRC bits		40		bits
Position bits (D31..D0)	**Left aligned**, unused LSB set 0		32		
Status bits	nE - not Error, active low nW - not Warning, active low		2		bits
CRC bits	Polynome: 0x43 ($X^6+X^1+X^0$) Start value: 0x00 Inverted before transmission		6		bits

The update of serial data occurs following the rising edge of the clock signal, and the bit must be latched at the subsequent falling edge of the clock signal. Position latching initiates with the first falling edge of the clock signal.



Time diagram for interface BIS20

It's worth noting that the BiSS-C specification provides comprehensive guidelines on line delay compensation, particularly useful for lengthy cable connections, allowing for adjustment in the timing of bit latching. For more detailed information, please refer to the official BiSS-C specification in Chapter "Line Delay" at the following link: https://biss-interface.com/.

2.4. BIS21: Serial interface *BiSS-C*

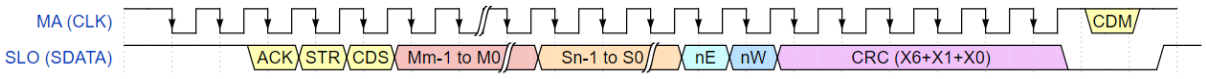
The BIS21 serves as an implementation of the bidirectional *BiSS-C* ® interface (a registered trademark of IC-Haus GmbH) and boasts the following key features:

- it reserves 32 bits for encoder position data
- the encoder position data is left-aligned, with unused lower bits/LSB set to 0

BIS20 is the recommended choice for rotary encoders with Multi Turn Option.

Parameter	Note	Min.	Typ.	Max.	Unit
Clock frequency		0.1		5.0	MHz
Processing time	ACK bit length = 1 clock (real time encoder)		0		µs
Total number of bits	Incl. Position, Status, CRC bits		40		bits
Multi Turn bits number	MT bits: M_{m-1} to M_0		m	12	bits
Multi Turn bits number	ST bits: S_{n-1} to S_0 (**left aligned**)		32-m		bits
Status bits	nE - not Error, active low nW - not Warning, active low		2		bits
CRC bits	Polynome: 0x43 ($X^6+X^1+X^0$) Start value: 0x00 Inverted before transmission		6		bits

The update of serial data occurs following the rising edge of the clock signal, and the bit must be latched at the subsequent falling edge of the clock signal. Position latching initiates with the first falling edge of the clock signal.



Time diagram for interface BIS21

This interface is recommended for encoders with the option “M” - Virtual Multi-Turn. Please add it in the ordering code of the product.

This interface can be ordered also for purely single turn encoders. In that case the encoder will count also the number of turns but it will reset the number of turns after power off.

Please contact FLUX in case you need support in choosing the right interface and ordering code for your product.

It's worth noting that the BiSS-C specification provides comprehensive guidelines on line delay compensation, particularly useful for lengthy cable connections, allowing for adjustment in the timing of bit latching. For more detailed information, please refer to the official BiSS-C specification in Chapter "Line Delay" at the following link: https://biss-interface.com/.

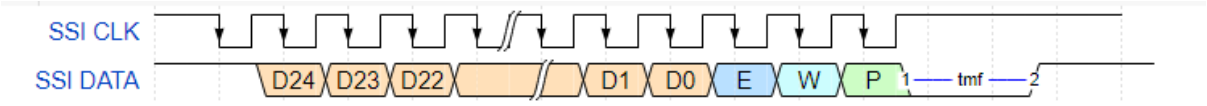
3. SSI Interfaces

3.1. SSI00: Serial interface SSI

The Synchronous Serial Interface (SSI) serves as a one-way communication channel, enabling the synchronized transmission of sensor output data, denoted as SSI DATA. This synchronization is achieved through the utilization of a shared clock signal SSI CLOCK. Both the DATA and CLOCK signals adhere to the RS-485 (EIA-485) standard, and they are transmitted using RS-485 line drivers.

Parameter	Notes	Min.	Typ.	Max.	Unit
Clock frequency		0.2		1.0	MHz
Monoflop time t_{mf}		30			µs
Total number of bits	Including position and status		28		bits
Number of data bits	D24 to D0 (**Right aligned**)		25		bits
Data alignment	Unused MSB set LOW-"0"	right aligned			
Number of status bits *S*	Error *E* (active high) Warning *W* (active high) Parity P (even)		3		bits

The onset of data transmission and position latching initiates with the first falling edge of the clock signal. The update of serial data occurs following the rising edge of the clock signal, and the bit must be latched at the subsequent falling edge of the clock signal.



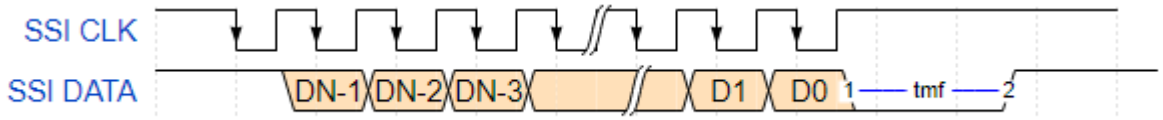
Time diagram for the SSI00 interface

3.2. SSI01: Serial interface SSI

The Synchronous Serial Interface (SSI) serves as a one-way communication channel, enabling the synchronized transmission of sensor output data, denoted as SSI DATA. This synchronization is achieved through the utilization of a shared clock signal SSI CLOCK. Both the DATA and CLOCK signals adhere to the RS-485 (EIA-485) standard, and they are transmitted using RS-485 line drivers.

Parameter	Notes	Min.	Typ.	Max.	Unit
Clock frequency		0.1		2.0	MHz
Monoflop time t_{mf}		20			µs
Number of data bits	Only position bits transmitted		N		bits
Data alignment		not relevant			
Number of status bits *S*	No status bit is transmitted		0		bits

The onset of data transmission and position latching initiates with the first falling edge of the clock signal. The update of serial data occurs following the rising edge of the clock signal, and the bit must be latched at the subsequent falling edge of the clock signal.



Time diagram for the SSI01 interface

3.3. SSI02: Serial interface SPI/SSI

The SSI02 configuration of the Synchronous Serial Interface SSI is compatible for establishing communication with a Serial Peripheral Interface (SPI) controller.

Synchronization of the sensor output signal, SSI DATA, is achieved through the shared SSI CLOCK signal. The transmission of both DATA and CLOCK signals adheres to the RS-485 (EIA-485) standard and is facilitated by RS-485 line drivers.

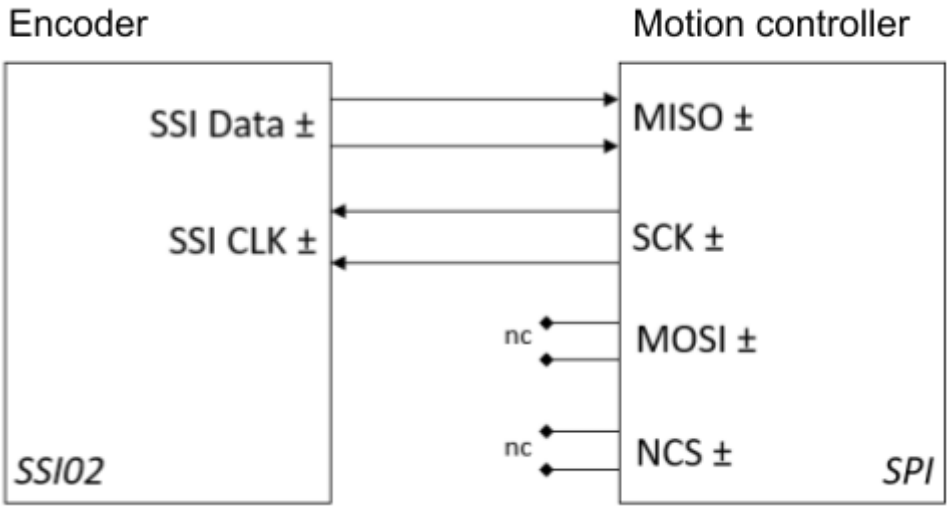


Fig.5.3.: Interfacing for SSI02 interface to the SPI master.

To interface with the SSI02, the following connections are necessary:

- Connect SSI Data to the SPI Master Input, Slave Output (MISO).
- Connect SSI Clock to the SPI Serial Clock (SCK).

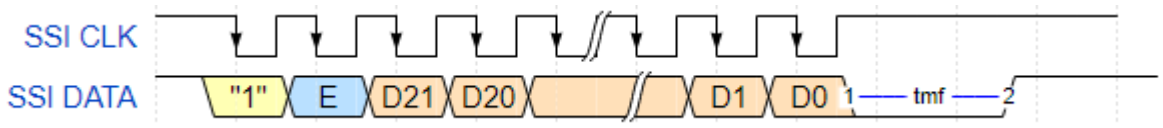
In this configuration, the SPI lines Master Output, Slave Input (MOSI), and SPI Not Chip Select (NCS) remain unconnected. In this setup, the encoder remains continuously enabled and provides the current position as a response.

SSI02 exclusively supports SPI Mode #2. The necessary SPI configuration for Mode #2 is as follows:

CPOL = ‘1’	SPI Clock (SCK) Idle Polarity is “1” / High
CPHA = ‘0’	SPI Data (MISO) is received/sampled on falling edge of the clock

The onset of data transmission and position latching initiates with the first falling edge of the clock signal. The update of serial data occurs following the rising edge of the clock signal, and the bit must be latched at the subsequent falling edge of the clock signal.

Parameter	Notes	Min.	Typ.	Max.	Unit
Clock frequency		0.2		1.0	MHz
Monoflop time t_{mf}		30			µs
Total number of bits			24		bits
Number of data bits	D21 to D0		22		bits
Data alignment	Unused MSB set LOW-”0”	right aligned			
Number of status bits *S*	Error *E* (active high)		1		bits



Time diagram for the SSI02 interface

Bits conversion for the 24 bits (23 down to 0) for the SPI master:

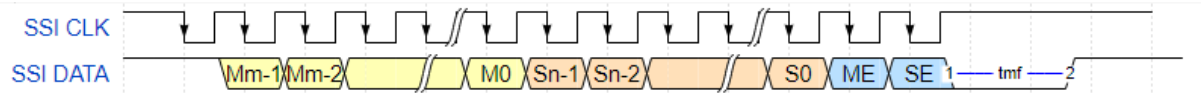
Bit		Description
Reserved	23 (MSB)	Bit always on “1”
Status	22	Error bit (active high) ‘0’ position valid / ‘1’ encoder error
Data bits	21… 0 (LSB)	Position, right aligned. Unused MSB bits set on ‘0’

3.4. SSI03: Serial interface SSI

The Synchronous Serial Interface (SSI) serves as a one-way communication channel, enabling the synchronized transmission of sensor output data, denoted as SSI DATA. This synchronization is achieved through the utilization of a shared clock signal SSI CLOCK. Both the DATA and CLOCK signals adhere to the RS-485 (EIA-485) standard, and they are transmitted using RS-485 line drivers.

Parameter	Note	Min.	Typ.	Max.	Unit
Clock frequency	data updated on rising clock edge	0.1		2.0	MHz
Monoflop time t_{mf}		20			µs
Total number of bits	MT bits + ST bits		m+n+2	46	
Multi Turn bits number	MT bits: M_{m-1} to M_0		m	12	bits
Multi Turn bits number	ST bits: S_{n-1} to S_0		n	32	bits
Data alignment		not relevant			
Number of status bits *S*	***ME*** Multi-Turn Error: active high ***SE*** Single-Turn Error: active high		2		bits

The data transmission and position latch starts with the first falling edge of the clock signal. The serial data update occurs on the rising clock edge.



Time diagram for the SSI03 interface

This interface is recommended for encoders with the option “M” - Virtual Multi-Turn. Please add it in the ordering code of the product.

This interface can be ordered also for purely single turn encoders. In that case the encoder will count also the number of turns but it will reset the number of turns after power off.

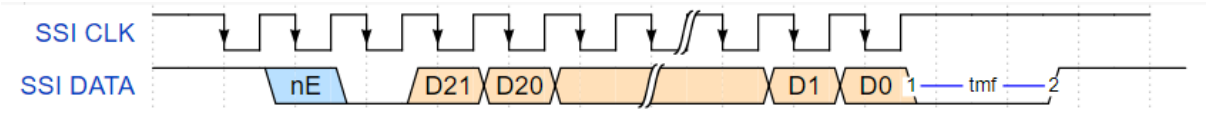
Please contact FLUX in case you need support in choosing the right interface and ordering code for your product.

3.5. SSI04: Serial interface SSI

The Synchronous Serial Interface (SSI) serves as a one-way communication channel, enabling the synchronized transmission of sensor output data, denoted as SSI DATA. This synchronization is achieved through the utilization of a shared clock signal SSI CLOCK. Both the DATA and CLOCK signals adhere to the RS-485 (EIA-485) standard, and they are transmitted using RS-485 line drivers.

Parameter	Note	Min.	Typ.	Max.	Unit
Clock frequency		0.1		2.0	MHz
Monoflop time t_{mf}		20			µs
Total number of bits			24		bits
Number of data bits	D21 to D0		22		bits
Data alignment	Unused MSB set LOW-”0”	right aligned			
Number of status bits *S*	Not Error n*E* (active low)		1		bits

The data transmission and position latch starts with the first falling edge of the clock signal. The serial data update occurs on the rising clock edge.



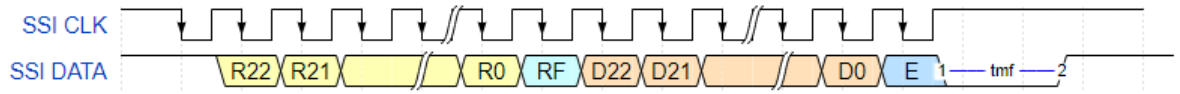
Time diagram for the SSI04 interface

3.6. SSI20: Serial interface SSI

The Synchronous Serial Interface (SSI) serves as a one-way communication channel, enabling the synchronized transmission of sensor output data, denoted as SSI DATA. This synchronization is achieved through the utilization of a shared clock signal SSI CLOCK. Both the DATA and CLOCK signals adhere to the RS-485 (EIA-485) standard, and they are transmitted using RS-485 line drivers.

Parameter	Note	Min.	Typ.	Max.	Unit
Clock frequency	data updated on rising clock edge	0.1		2.0	MHz
Monoflop time t_{mf}		20			µs
Total number of bits			48		bits
Position Referenced bits	R22 to R0 (signed, 2's complement)		23		bits
Referenced Flag bits	"1" referenced		1		bits
Position Not-referenced bits	D22 to D0 (signed, 2's complement)		23		bits
Status bits	E - error active on "1"		1		bits

The data transmission and position latch starts with the first falling edge of the clock signal. The serial data update occurs on the rising clock edge.



Time diagram for the SSI20 interface

After power-on, the **Position Not-Referenced** starts from a 'near-zero' position (it is the position inside of the scale pitch) and counts in a positive or negative direction. The representation of the data is done in 2's complement, with 1 bit representing one resolution increment. This counter will count continuously and will not be affected by crossing the reference.

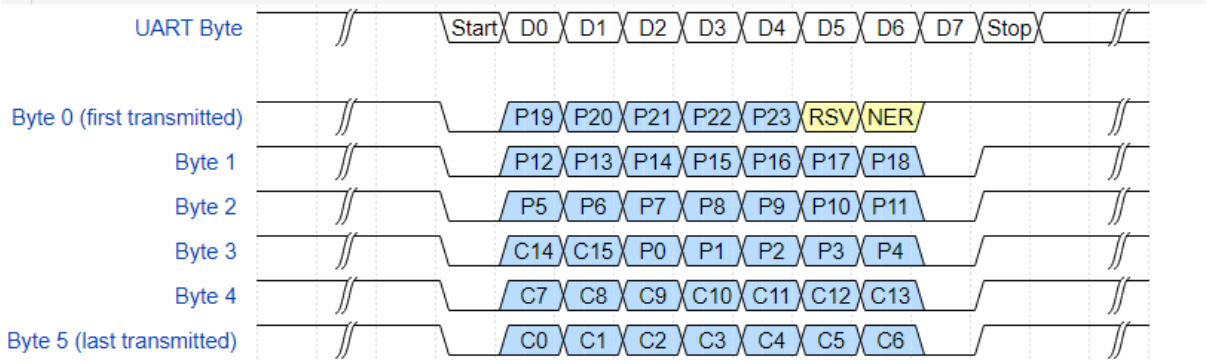
The second position, the **Position Referenced**, stays on 0 as long as the reference mark is not crossed. As soon as the reference mark is crossed for the first time, the RF (referenced flag) will be set to '1,' and the position will start to count in 2's complement relative to it.

4. UART Interfaces

4.1. UATxx: Universal Asynchronous Transmitter

The UATxx interface utilizes the simplified UART specification to transmit data. It is a unidirectional interface, comprising one TX line. The physical layer employed for data transmission is RS485/RS422, which employs a differential TX± line.

Data is transmitted continuously, with each full frame consisting of 6 Bytes.
The format of each byte within the frame is as follows: it begins with a Start bit (0/Low), followed by 7 data bits (LSB sent first), and concludes with a Stop bit (1/High). To identify the first byte (Byte 0) in a frame, the bit D7 is exclusively set to 1 for the initial Byte 0, while all the other Bytes terminate with D7 as 0.



Time diagram for the UATxx interface

NER (No Error Bit)	NER indicates whether there is an error or not. '0' represents an error, while '1' indicates a valid position value.
RSV (Reserved)	Reserved and always set to 0.
P[23 .. 0] (Position Bits)	24 bits represent the position data, right-aligned. When the resolution is lower than 24 bits, the upper/MSB bits remain unused.
C[15 .. 0] (CRC / Cyclic Redundancy Check)	16-bit CRC used for error checking in the frame. CRC polynomial = 0x8005, CRC start value = 0x0000. Not reversed and not inverted during computation.

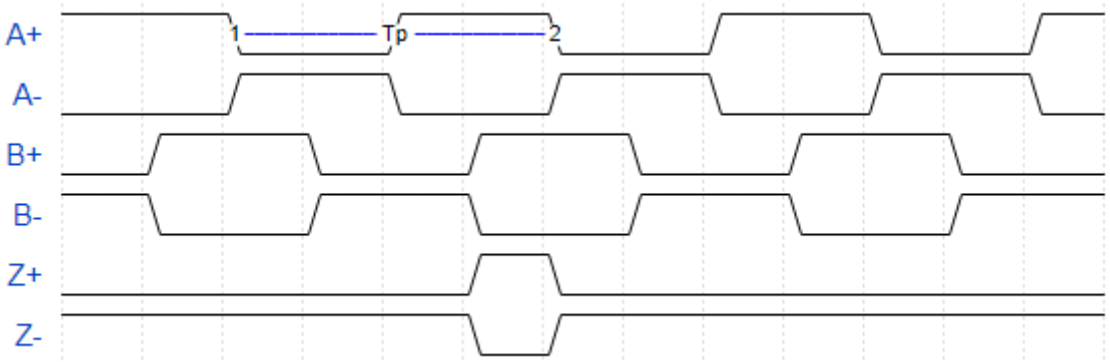
Two baud rates and frames cycles are available:

UATxx	**Baud rate**	**Frame cycle**
UAT00	230’400 bps	2.5 kHz
UAT01	921’600 bps	10 kHz

5. Quadrature interface

5.1. INCxx: Quadrature output

The incremental quadrature output comprises two square-wave position signals, denoted as A and B, which are differentially encoded and exhibit a 90° phase shift relative to each other. Additionally, a differential square-wave Reference Index pulse (Z) is provided for use in homing procedures.



Time diagram for interface INCxx with differential TTL quadrature signal

The maximum frequency of the signals is determined by taking the inverse of the minimum period of one cycle that can be outputted by the encoder. Subsequently, after x4 decoding, the maximum number of encoder counts that can be outputted is obtained.

INCxx	**Maximum output cycle (1/Tp) Before x4 decoding**	**Maximum output counts After x4 decoding**
INC00	5.000 MHz	20.0 Mio. / sec
INC01	2.500 MHz	10.0 Mio. / sec
INC02	1.250 MHz	5.0 Mio. / sec
INC03	0.625 MHz	2.5 Mio. / sec

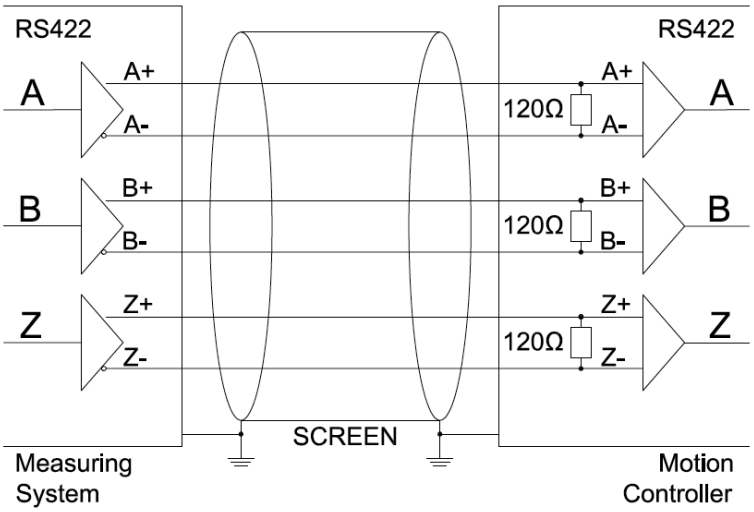
The maximum operating speed of the encoder may be reduced from the standard maximum of 10 m/s due to the selection of higher resolutions or lower clock speeds. Maximum speed is computed using the following formula but is in no case more than 6000 rpm:

$$Maximum\ speed\ [rpm] = 60 \times \frac{4\ x\ Maximum\ Output\ Frequency\ [Hz]}{2^{\ Encoder\ resolution\ [bit]}\ [1/rev]}$$

For example purposes, the maximum encoder speed has been calculated for two different resolutions (18 bits/rev and 14 bits/rev) across various output frequencies

Interface	Max. Frequency (before x4)	Max. Counts (after x4)	Maximum speed	
			@ 18 bits/rev	@ 14 bits/rev
INC00	5.000 MHz	20.0 Mio. / sec	4577 rpm	6000 rpm
INC01	2.500 MHz	10.0 Mio. / sec	2288 rpm	6000 rpm
INC02	1.250 MHz	5.0 Mio. / sec	1144 rpm	6000 rpm
INC03	0.625 MHz	2.5 Mio. / sec	572 rpm	6000 rpm

Below are the recommended line driver and line termination options:



Recommended electrical connection

6. Revision history

Date	Version	Comments
2023-11	00	First built - based on the interfaces previous described in IND-ROT, GMI-ROT, GMI-ANG datasheets
2024-02	01	SSI03 total number of bits corrected. Selection matrix corrected. Links in document updated. Position of nError and nWarning corrected for BiSS-C interface.

Technical data is subject to change without notice.

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